TITLE OF THE INVENTION

# Liquid Crystal Display Apparatus and Method of Driving LCD Panel

## BACKGROUND OF THE INVENTION

### Field of the Invention

The present invention relates to a liquid crystal display apparatus and a method of driving a liquid crystal display panel.

### Description of the Related Art

A liquid crystal display panel comprises a matrix array of pixels each being formed by a switching transistor and a liquid crystal cell. All switching transistors are connected to intersections of column lines and row lines which are successively selected. When one of the row lines is selected, the column lines are respectively driven by write-in voltages. With the advancing technology in the field of flat panel displays, the recent tendency is toward developing large sized, high definition display panels. As the screen size increases, the write-in voltages must travel through the increased length of the column lines. Since the write-in voltages are supplied to the liquid crystal cells of the selected row line for a fixed write-in period, they suffer from undesirable attenuation and distortion, causing different shades of gray to occur between the top and bottom of the screen as illustrated in Fig. 1.

To overcome this problem, Japanese Patent Publication 2002-182616 discloses a technique whereby variable supplemental voltages are generated and combined with write-in voltages. The combined voltages vary increasingly with the distance between the selected row line to the end points where the combined voltages are supplied.

However, because of the analog circuitry, difficulty arises to provide precision circuit adjustment. Therefore, a need exists to provide a solution whereby circuit adjustment can be easily and precisely performed on liquid crystal display apparatus.

## SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide a liquid

crystal display apparatus and a method of driving a liquid crystal display panel by controlling the write-in period according to different distances traveled along the column lines by the write-in voltages. Since the pulse duration can be easily controlled by digital circuitry, the present invention solves the problem of different shades of gray across the screen of a liquid crystal display.

According to a first aspect of the present invention, there is provided a liquid crystal display apparatus comprising a liquid crystal display panel a liquid crystal display panel comprising a matrix array of transistors and a matrix array of liquid crystal cells respectively connected to the transistors, the transistors being respectively connected to intersections of a plurality of column lines and a plurality of row lines for activating the liquid crystal cells, and a driving circuit for successively generating a plurality of write-in voltages of a line signal of a video frame at end points of the column lines, successively selecting each of the row lines and supplying the write-in voltages from the end points of the column lines to the liquid crystal cells of the selected row line for a variable write-in period corresponding to a geometric distance from the selected row line to the end points. The write-in period may be increasingly variable from a nominal value or increasingly variable from a less-than-nominal value to the nominal value or a combination of both.

According to a second aspect, the present invention provides a method of driving a liquid crystal display, wherein the liquid crystal display panel comprises a matrix array of transistors and a matrix array of liquid crystal cells respectively connected to the transistors, the transistors being respectively connected to intersections of a plurality of column lines and a plurality of row lines for activating the liquid crystal cells. The method comprises the steps of (a) generating a plurality of write-in voltages of a line signal of a video frame so that the write-in voltages appear at end points of the column lines, (b) successively selecting one of the row lines, and (c)

successively supplying the write-in voltages from the end points of the column lines to the liquid crystal cells of the selected row line for a write-in period corresponding to the geometric distance from the selected row line to the end points.

## BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be described in detail further with reference to the following drawings, in which:

Fig. 1 is a graphic representation of a prior art liquid crystal display panel in which luminance values are plotted as a function of time to illustrate a luminance error between the first and last lines;

Fig. 2 is a block diagram of an LCD drive circuit according to a first embodiment of the present invention;

Fig. 3 is a block diagram of the timing controller of Fig. 2;

Fig. 4 is a timing diagram of the operation of Fig. 3;

Fig. 5 is a graphic representation of the luminance-versus-time characteristics of the first embodiment of the present invention;

Fig. 6 is a block diagram of an LCD drive circuit according to a second embodiment of the present invention;

Fig. 7 is a block diagram of the timing controller of Fig. 6;

Fig. 8 is a timing diagram of the operation of Fig. 6;

Fig. 9 is a graphic representation of the luminance-versus-time characteristics of the second embodiment of the present invention;

Fig. 10 is a block diagram of an LCD drive circuit according to a third embodiment of the present invention;

Fig. 11 is a block diagram of the timing controller of Fig. 10;

Fig. 12 is a timing diagram of the operation of Fig. 10; and

Fig. 13 is a graphic representation of the luminance-versus-time characteristics of the third embodiment of the present invention.

## DETAILED DESCRIPTION

Referring now to Fig. 2, there is shown an LCD drive circuit according

to a first embodiment of the present invention. The drive circuit comprises a column driver 2 and a row driver 3 for respectively driving a liquid crystal display panel 1 in response to timing pulses supplied from a timing controller 4. In the first embodiment, the vertical blanking interval of each frame is utilized to stretch gate control pulse longer than the usual gate-on time. For this purpose, a buffer memory 5 is provided for temporarily storing video input data from an external source, not shown. The stored video data is supplied line-by-line to the column driver 2. Input timing signal (sync and clock) is also supplied from the external source to the timing controller 4.

The LCD panel 1 is comprised of a plurality of column (drain) lines 10 connected to the column driver 2 for receiving video signals, a plurality of horizontal row (gate) lines 11-1 ~ 11-N connected to the row driver 3 for receiving a gate control pulse. A matrix array of picture elements (pixels) are located at intersections of the column lines 10 and the row lines 11. Each pixel comprises a thin-film transistor 12 and a liquid crystal cell 13. In each pixel, the transistor 12 connects its drain to the associated column line 10 and its gate to the associated row line 11, and the liquid crystal cell 13 is connected between the source of the transistor 12 and a common electrode 14.

As will be described below, the gate control pulse is shifted from one row line to the next in response to a gate drive clock pulse (VCK) from the timing controller 4. The duration of each gate control pulse begins at the leading edge of a VCK pulse and ends at the leading edge of the next VCK pulse. In the presence of a gate control pulse, a line signal of a video frame supplied to the column driver 2 is latched in response to a data latch pulse (DLP). A "write-in period" of a selected row line is defined between the trailing edge of a DLP pulse and the leading edge of a VCK pulse for writing the latched line signal into the liquid crystal cells 13 of a selected row line 11. By increasing varying the interval between successive VCK pulses according to the geometric distance from a selected row line to the column driver 2 along the column lines 10, the write-in period is increasingly varied as the

point of selection proceeds from the row line 11-1 to the row line 11-N.

All liquid crystal cells 13 are air-tightly sealed in a transparent flat panel, not shown, and the column lines 10, the row lines 11 and the transistors 12 are arranged on one side of the flat panel and the common electrodes 14 and a color filter are arranged on the other side. Each liquid crystal cell 13 corresponds in position to each dot of the screen and is capable of charging a "write-in" voltage supplied from the column driver 2 when the associated switching transistor 12 is turned on in response to a gate control pulse from the row driver 3. When the transistor 12 is turned off at the trailing edge of the gate control pulse, the associated liquid crystal cell 13 holds the write-in voltage until the end of a frame period.

All the common electrodes 14 are usually biased at a constant voltage of 7 volts. Using this bias voltage as a reference, the polarity of the write-in voltage is determined. Usually, a positive write-in voltage varies in the range between 8 and 13 volts and a negative write-in voltage varies in the range between 1 and 6 volts. Thus, the write-in voltage varies in a range from 1 to 6 volts on either side of the 7-volt reference voltage.

In the first embodiment, the column driver 2, also known as a source driver, includes a shift register 20, a latch circuit 21 and a conversion circuit 22. Shift register 20 responds to a start pulse (SP) from the timing controller 4 for receiving video data which is serially clocked pixel-by-pixel in response to a dot clock pulse (DCK). When all pixel data of a line are clocked into the shift register 20, they are supplied in parallel to the latch circuit 21 in response to the leading edge of a data latch pulse (DLP) from the timing controller 4. Conversion circuit 22 performs the conversion of individual pixel data into write-in voltages and drives the column lines 10 with the write-in voltages via appropriate impedance matching circuits.

Row driver 3, which is also known as a gate driver which responds to the start pulse (SP) and a gate-drive clock pulse (VCK) from the timing controller 4 for sequentially selecting the row lines 11-1 ~ 11-N so that each

row line is selected between the leading edge of the corresponding VCK pulse and the leading edge of the next VCK pulse. For each row line 11-i (i=1, 2, ...N), each of the SP, VCK and DLP pulses is generated at intervals increasingly variable as a function of the geometric distance along the column lines 10 from the selected row line 11-i to the column driver 2.

As shown in Fig. 3, the timing controller 4 of the first embodiment comprises a sync detector 40 for discriminating the input clock and sync timing signals to detect the frame sync and line sync timing of the input video frame and produces a dot clock pulse DCK. A line counter 41, which is reset when a frame sync is detected, increments a count number each time a line sync is detected and provides a binary line-count number to a memory 42. Write-in additive timing values 0, $\alpha_1$ through $\alpha_{N-1}$ are stored in the memory 42, respectively corresponding to row lines 11-1, 11-2 through 11-N. Each of the additive timing values $\alpha_1$ through $\alpha_{N-1}$ is determined as a function of the geometric distance from a corresponding one of the row lines 11-2 ~ 11-N to the column driver 2 along the column lines 10. Note that the total number of DCK pulses assigned to these additive timing values is equal to (M - N) x G, where M - N is the number of lines which can be generated within the vertical blanking interval and G is the number of DCK pulses during each line interval.

Each additive variable is read from the memory 42 in response to a corresponding line-count number and supplied to an adder 43 where the additive variable is summed with an integer X, where X is the nominal value of the write-in period. The binary output of the adder 43 is connected to a variable rate pulse generator 44. This variable rate pulse generator may be implemented with a presettable counter which increments a count number in response to the DCK pulse and produces an output when that count number equals some preset value, which is set equal to the output of adder 43. Variable rate pulse generator 44 produces SP, VCK and DLP pulses, each of which occurs at intervals varying increasingly as the row lines 11-1 ~ 11-N

are selected in sequence in that order. All of these variable-rate pulses have a fixed time difference from one another. Initially, the variable rate pulse generator 44 is activated to produce a first VCK pulse when the sync generator 40 detects a frame sync.

The variable-rate SP and VCK pulses are supplied to the row driver 3 and the variable-rate SP and DLP (data latch) pulses are supplied to the column driver 2 along with constant-rate DCK (dot clock) pulse which is supplied from the sync detector 40. The SP and DCK pulse are also supplied from the timing controller 4 to the buffer memory 5 so that stored video data can be read line-by-line into the column driver 2 when a row line is selected.

The operation of the first embodiment of the present invention is best understood with the following description with reference to the timing diagram of Fig. 4.

As shown in Fig. 4, a frame interval is divided into a vertical scan interval and a vertical blanking interval. During the vertical scan interval, each of the #1 to #N line signal of a video frame is sequentially read into the buffer memory 5.

In response to a variable-rate start pulse SP, a line signal is read out of the buffer memory 5 and clocked into the column-driver shift register 20 and stored in the latch circuit 21 in response to a variable-rate DLP pulse. Row driver 3 selects one of the row lines 11-i in response to the same start pulse and generates a gate control pulse in response to a variable-rate VCK pulse to drive the selected row line 11-i. In this way, the row lines 11-1 through 11-N are successively rendered active for periods $T_1$, ...., $T_N$.

In the prior art, the write-in period is fixed at the nominal interval (X) for all row lines. As shown in Fig. 5, the write-in periods of row lines 11-1, 11-2, ....., 11-N are respectively set equal to X, $X + \alpha_1$, ....., $X + \alpha_{N-1}$. As a result, the distance-associated different voltage drops along the column lines 10 is compensated. For a given write-in voltage, the light intensities of all liquid crystal cells 10 are rendered substantially equal to each other.

Since the pulse interval can be easily controlled by the use of the digital circuitry, the variable intervals of the SP, DLP and VCK pulses can be precisely controlled to eliminate the undesired differences in shades of gray between the top and bottom lines on the monitor screen. The precision timing control is particularly important since the time assigned for each write-in operation is becoming increasingly limited with the current tendency toward developing high resolution, large-screen displays.

A second embodiment of the present invention is shown in Fig. 6. In this embodiment, the write-in operations of the row lines 11-1 to 11-N are respectively performed within periods $T_1 = X - \beta_1$, $T_2 = X - \beta_2$, ...., $T_{N-1} = X - \beta_{N-1}$, and $T_N = X$, where $\beta_1 \geq \beta_2 \geq$ ....., $\beta_{N-2} \geq \beta_{N-1}$, and $\beta_i$ (i = 1, ...., N - 1) is a subtractive timing value which varies decreasingly as a function of geometric distance along the column lines between the row line 11-i and the column driver 2. Therefore, the write-in period $T_i = X - \beta_i$ varies increasingly, within the nominal write-in period X, as a function of the geometric distance along the column lines between the row line 11-i and the column driver 2. The write-in operation is thus performed within an interval smaller than the horizontal line interval of the input video frame.

Since the write-in operation of the liquid crystal elements 13 does not take longer than the time for writing the input line data into the shift register 20, the buffer memory of the previous embodiment is not necessary in this embodiment.

In the second embodiment, VCK and DLP pulses are generated at constant intervals and a video output enable (VOE) pulse is generated at intervals increasingly variable as a function of the geometric distance from the row lines to the column driver 2. In the row driver 3, each gate control pulse is generated so that its begins in response to the constant-rate VCK pulse and ends in response to the VOE pulse.

As shown in detail in Fig. 7, the timing controller 4 of the second embodiment comprises a sync detector 50 for discriminating the input clock

and sync timing signals to detect the frame sync and line sync timing of the input video frame and the dot clock pulse DCK. A constant-rate pulse generator 51 responds to the detected frame and line sync timing for producing a start pulse (SP), a DLP pulse and a VCK pulse at constant intervals. A line counter 52, which is reset by a frame sync, increments a count number each time a line sync is detected and provides a binary line-count number to a memory 53. Write-in subtractive timing values $\beta_1$ through $\beta_{N-1}$ and "0" are stored in the memory 53 respectively corresponding to row lines 11-1, ....., 11-N-1, and 11-N.

Each subtractive timing value is read from the memory 53 in response to a corresponding line-count number and supplied to a subtractor 54 where the subtractive timing value is subtracted from the nominal value X. The binary output of the subtractor 54 is then used to preset a variable rate pulse generator 55. Variable rate pulse generator 55 responds to a constant-rate VCK pulse by starting the count of DCK pulses and generates a VOE pulse when the count number equals the preset value.

The variable-rate VOE pulse and the constant rate SP and VCK pulses are supplied to the row driver 3 and the constant-rate SP and DLP pulses are supplied to the column driver 2 along with the input video frame (data) and DCK pulse.

The operation of the second embodiment of the present invention proceeds according to the timing diagram of Fig. 8.

When a line signal of the input video frame is clocked into the column driver 2 in response to a constant-rate start pulse SP and latched in response to a DLP pulse, the row driver 3 selects a row line 11-i and generates a gate control pulse in response to a VCK pulse to drive the selected row line. This gate control pulse terminates in response to a subsequent VOE pulse so that the write-in period $T_i$ for the row line 11-i is equal to $X - \beta_i$, which begins at the trailing edge of the DLP pulse and ends at the leading edge of the VOE pulse. In this manner, the row lines 11-1 through 11-N are successively

selected and rendered active for write-in periods $T_1$, ...., $T_N$, respectively. The distance-related different voltage drops along the column lines are compensated and all liquid crystal cells are charged with substantially equal voltages regardless of their relative positions to the column driver 2, as graphically shown in Fig. 9.

A third embodiment of the present invention is shown in Fig. 10. This embodiment is a combined form of the previous embodiments. Accordingly, the timing controller 4 of the third embodiment is of similar configuration to that of Fig. 3 modified according to Fig. 7.

As illustrated in Fig. 11, the timing controller of the third embodiment comprises sync detector 60 for discriminating the input clock and sync timing signals to detect the frame sync and line sync timing of the input video frame and the dot clock pulse DCK. Constant-rate pulse generator 61 responds to the detected frame and line sync timing for producing SP1, DLP1 and VCK1 pulses at constant intervals. Line counter 62, which is reset by a frame sync, increments a count number each time a line sync is detected and provides a binary line-count number to a memory 63. Write-in subtractive timing values $\beta_1$, $\beta_2$,....., $\beta_{M-1}$ and write-in additive timing values 0, $\alpha_{M+1}$, $\alpha_{M+2}$, ....., $\alpha_{N-1}$ are stored in the memory 63 respectively corresponding to row lines 11-1, 11-2, ...., 11-M-1, 11-M, 11-M+1, 11M+2, ....., 11-N.

During a first portion of each video frame, each subtractive timing value is read from the memory 63 in response to a corresponding line-count number and supplied to a subtractor 64 where the subtractive timing value is subtracted from the nominal value X. The binary output of the subtractor 64 is used to preset a variable rate pulse generator 66. Variable rate pulse generator 66 responds to a constant-rate VCK1 pulse by starting the count of DCK pulses and generates a variable-rate VOE pulse when the count number equals the preset value. The variable-rate VOE pulse and the constant rate SP1 and VCK1 pulses are supplied to the row driver 3 and the constant-rate SP1 and DLP1 pulses are supplied to the column driver 2 along with the

input video frame (data) and DCK pulse. Buffer memory 5 is supplied with the DCK pulse and the constant-rate start pulse SP1.

During a second portion of the video frame, each additive timing value is read from the memory 63 in response to a corresponding line-count number and supplied to an adder 65 where the additive timing value is summed with the nominal value X. The binary output of the adder 65 is used to preset the variable rate pulse generator 66. When the preset value is reached, the variable rate pulse generator 66 produces pulses SP2, DLP2 and VCK2 at variable intervals, instead of the VOE pulse. The variable-rate SP2, and VCK2 pulses are supplied to the row driver 3 and the SP2 and DLP2 pulses are supplied to the column driver 2 along with the input video frame and DCK pulse. Buffer memory 5 is supplied with the DCK pulse and the variable-rate start pulse SP2.

The operation of the third embodiment of the present invention proceeds according to the timing diagram of Fig. 12.

During the first portion of a frame interval, each line signal of the input video frame is clocked into the column driver 2 in response to a constant-rate start pulse SP1 and latched in response to a DLP1 pulse, and the row driver 3 selects a row line 11-i and generates a gate control pulse in response to a constant-rate VCK1 pulse to drive the selected row line. This gate control terminates in response to a subsequent VOE pulse so that the write-in period $T_i$ is equal to $X - \beta_i$. In this manner, the row lines 11-1 through 11-M-1 are successively selected and rendered active for write-in periods $T_1, \ldots, T_{M-1}$, respectively.

During the second portion of the frame interval, each line signal of the input video frame is clocked into the column driver 2 in response to a variable -rate start pulse SP2 and latched in response to a variable-rate DLP2 pulse, the row driver 3 selects a row line 11-i and generates a gate control pulse in response to a variable-rate VCK2 pulse to drive the selected row line. This gate control pulse terminates in response to a subsequent VCK2 pulse so

that the write-in period $T_i$ is equal to $X - \alpha_i$. In this manner, the row lines 11-M through 11-N are successively selected and rendered active for write-in periods $T_M$, ...., $T_N$, respectively.

As shown in Fig. 13, the write-in periods for row lines 11-1 to 11-M-1 are $T_1 = X - \beta_1$, $T_2 = X - \beta_2$,...., $T_{M-1} = X - \beta_{M-1}$, respectively, and the write-in periods for row lines 11-M to 11-N are $T_M = X$, $T_{M+1} = X + \alpha_1$, ....., $T_N = X + \alpha_{N-1}$, respectively, where $\beta_1 \geq \beta_2 \geq$,..... $\geq \beta_{M-1}$ and $\alpha_1 \leq \alpha_2 \leq$ ..., $\alpha_{N-2} \leq \alpha_{N-1}$.